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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/989,762	11/19/2001	Kenneth Y. Ogami	CYPR-CD01175M	2087

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EXAMINER	
OSBORNE, LUKE R	

ART UNIT	PAPER NUMBER
2123	

DATE MAILED: 07/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/989,762	OGAMI ET AL.	
	Examiner	Art Unit	
	Luke Osborne	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 February 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 November 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Status

1. Claims 1-33 are pending in the instant application.

Claims 1-33 stand rejected.

Drawings

2. Figures 1-5 are objected to by the Draftsperson under 37 CFR 1.84 or 1.152 for the reason(s) attached on form PTO-948.

Abstract

3. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

The abstract of the disclosure is objected to because it is over 150 words. Correction is required. See MPEP § 608.01(b).

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

4. Claims 1-14 rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

For a claimed invention to be statutory, the claimed invention must be within the technological art. Mere ideas in the abstract (i.e., abstract idea, law of nature, natural phenomena) that do not apply, involve, use, or advance the technological art fail to promote the "progress of science and the useful arts" (i.e., the physical sciences as opposed to social sciences, for example) and therefore are found to be non-statutory subject matter. For a method claim to pass muster, the recited process must somehow apply, involve, use, or advance the technological arts.

As to technological arts recited in the preamble, mere recitation in the preamble (i.e., intended or field of use) or mere implication of employing a machine or article of manufacture to perform some of the recited steps does not confer statutory subject matter to an otherwise abstract idea unless there is positive recitation in the claim as a whole to breathe life and meaning into the preamble. In Bowman (Ex parte Bowman, 61 USPQ2d 1665, 1671 (BD. Pat. App. & Inter. 2001) (Unpublished), the board affirmed the rejection under U.S.C. 101 as being directed to non-statutory subject matter. Although Bowman discloses transforming physical media into a chart and physically plotting a point on said chart, the Board held that the claimed invention is nothing more than an abstract idea, which is not tied to any technological art or environment.

In the present case, although claim 1 recites at the preamble a method of utilizing a programmable plurality of resources on an integrated circuit, the steps in the claim

body of selecting a user module, comparing a description, and identifying a first allowed resource, can be implemented by the mind of a person or by the use of a pencil and paper. In other words, since the claimed invention, as a whole, is not within the technological arts as explained above, these claims only constitute an idea and does not apply, involve, use, or advance the technological arts, thus, it is deemed to be directed to non-statutory subject matter.

Any claim not directly rejected on 35 U.S.C 101 stands rejected due to its dependency.

To expedite a complete examination of the instant application, the claims rejected under 35 U.S.C 101(nonstatutory) above are further rejected as set forth below in anticipation of applicant amending these claims to place them within the four statutory categories of invention.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1, 4, 7, 8, 10-15, 18-24, 26- 32 rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Pre-Grant Publication No. 2002/0016706 to Cooke et al. hereafter, "Cooke."

Regarding claim 1, Cooke discloses a method of utilizing a programmable plurality of resources on an integrated circuit. See Figures 1, 2, 3 and the corresponding portions of Cooke's speciation for this disclosure. In particular, Cooke discloses "a method of utilizing a programmable plurality of resources on an integrated circuit comprising:

a. selecting a user module [block] representing an electronic design [From the HDL or other high level description, the actual logic cell implementation is typically determined by logic synthesis, which converts the functional description of the block into a specific circuit implementation of the block. (Paragraph 36)];

b. comparing a description of a hardware resource requirement of the user module with a description of the plurality of programmable resources on the integrated circuit [The computer 110 is preferably coupled to a mass storage device (e.g., magnetic disk or cartridge storage) providing a layout database 195 with which the foregoing system components interface (Paragraph 40)]; and

c. identifying a first allowed programmable hardware resource on the integrated circuit satisfying the hardware resource requirement of the user module [At each stage of the design process, as well as at the fabrication stage,

various tests may be run to ensure correct operability of the circuit design (Paragraph 36)]" as claimed.

Regarding claim 4, Cooke discloses the method according to Claim 1 "further comprising highlighting the first allowed programmable hardware resource using a graphical user interface

> [The block floorplanner 120 provides for the definition of block functions, block regions, and constraints on these for the purpose of interactive floorplanning operations by the circuit designer, and the control of placement operations of the block placer 130. The block placer 130 determines the placement of cells within blocks according to the constraints defined by the circuit designer. (Paragraph 38)]" as claimed.

Regarding claim 7, Cooke discloses the method according to Claim 1 "further comprising identifying a disallowed programmable resource on the integrated circuit wherein the disallowed resource represents an unavailable resource on the integrated circuit that otherwise satisfies the hardware resource requirement of the user module

> [The block floorplanner 120 provides for the definition of block functions, block regions, and constraints on these for the purpose of interactive floorplanning operations by the circuit designer, and the control of placement operations of the block placer 130. The block placer 130 determines the placement of cells within blocks according to the constraints defined by the circuit designer. (Paragraph 38)]" as claimed.

Regarding claim 8, Cooke discloses the method according to Claim 7 "further comprising highlighting the disallowed programmable resource using said graphical user interface

> [The block floorplanner 120 provides for the definition of block functions, block regions, and constraints on these for the purpose of interactive floorplanning operations by the circuit designer, and the control of placement operations of the block placer 130. The block placer 130 determines the placement of cells within blocks according to the constraints defined by the circuit designer. (Paragraph 38)]" as claimed.

Regarding claim 10, Cooke discloses the method according to Claim 1 "further comprising updating the description of the hardware resource requirement of the user module

> [Chip designers generally use a top-down design methodology, starting with hardware description languages (HDLs), such as Verilog.RTM. or VHDL, for example, to create an integrated circuit by hierarchically defining functional components of the circuit, and then decomposing each component into smaller and smaller components. (Paragraph 35)]" as claimed.

Regarding claim 11, Cooke discloses the method according to Claim 10 "wherein updating is performed in response to changes in a hardware resource requirement of the user module

> [Chip designers generally use a top-down design methodology, starting with hardware description languages (HDLs), such as Verilog.RTM. or VHDL, for example, to create an integrated circuit by hierarchically defining functional components of the circuit, and then decomposing each component into smaller and smaller components. (Paragraph 35)]" as claimed.

Regarding claim 12, Cooke discloses the method according to Claim 1 "further comprising adding an additional user module to the description of the hardware resource requirement of the user module [From the HDL or other high level description, the actual logic cell implementation is typically determined by logic synthesis, which converts the functional description of the block into a specific circuit implementation of the block. (Paragraph 36)]" as claimed.

Regarding claim 13, Cooke discloses the method according to Claim 1 "further comprising updating the description of the plurality of programmable resources on the integrated circuit

> [The block floorplanner 120 provides for the definition of block functions, block regions, and constraints on these for the purpose of interactive floorplanning operations by the circuit designer, and the control of placement operations of the block placer 130. The block placer 130 determines the placement of cells within blocks according to the constraints defined by the circuit designer. (Paragraph 38)]" as claimed.

Regarding claim 14, Cooke discloses the method according to Claim 13 "further comprising adding an additional chip description to the description of the plurality of resource on the integrated circuit

> [The block floorplanner 120 provides for the definition of block functions, block regions, and constraints on these for the purpose of interactive floorplanning operations by the circuit designer, and the control of placement operations of the block placer 130. The block placer 130 determines the placement of cells within blocks according to the constraints defined by the circuit designer. (Paragraph 38)]" as claimed.

Claim 15 recites the apparatus of method claim 1, thus is rejected for the same reasons as claim 1.

Claim 18 recites similar limitations as the method of claim 1, thus is rejected for the same reasons as claim 1.

Regarding claim 19, Cooke discloses the method according to Claim 18 "further comprising:

displaying on a graphical user interface, a first potential placement of said potential placement options; and in response to a user selecting a next placement icon, displaying on said graphical user interface, a second potential placement of said potential placement options [The block placer 130 determines the placement of cells

within blocks according to the constraints defined by the circuit designer. (Paragraph 38)]" as claimed.

Regarding claim 20, Cooke discloses the method according to Claim 19 "wherein potential placement options are displayed using visual attributes and wherein said electronic device is a programmable microcontroller device [Figure 2A Microcontroller item 200]" as claimed.

Regarding claim 21, Cooke discloses the method according to Claim 18 "wherein said user module requires one programmable resource to place [Figure 2A item B's]" as claimed.

Regarding claim 22, Cooke discloses the method according to Claim 18 "wherein said user module requires two programmable resources to place [Figure 2A item B's]" as claimed.

Regarding claim 23, Cooke discloses the method according to Claim 18 "wherein said plurality of programmable resources comprise a plurality of analog programmable resources and a plurality of digital programmable resources [The computer 110 may also comprise or be connected to mass storage containing one or more component libraries (not shown) specifying features of electrical components available for use in circuit designs (Paragraph 40)]" as claimed.

Regarding claim 24, Cooke discloses the method according to Claim 18 "wherein said comparing automatically prunes out programmable hardware resources that do not satisfy requirements of said user module

> [The block floorplanner 120 provides for the definition of block functions, block regions, and constraints on these for the purpose of interactive floorplanning operations by the circuit designer, and the control of placement operations of the block placer 130. The block placer 130 determines the placement of cells within blocks according to the constraints defined by the circuit designer. (Paragraph 38)]" as claimed.

Claims 26-32 recite the system of method claims 18-24, thus are rejected for the same reasons as claims 18-24

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 2, 3, 5, 6, 9, 16, 17, 25, 33 rejected under 35 U.S.C. 103(a) as being unpatentable over Cooke.

Regarding claim 2 Cooke teaches the method according to Claim 1 wherein the description of the hardware resource requirement of the user module is represented as data.

Cooke does not expressly teach that the data in the method takes the form of the XML data.

However, these differences from the prior art of record are only found in the nonfunctional descriptive material and do not make a meaningful contribution to the definition of the invention as recited. The limitation of XML does not alter how the method as described in the specification functions. Thus, the identified descriptive material will not distinguish the claimed invention from the prior art in terms of patentability, see In re Gulack, 703 F.2d 1381, 1385, 217 USPQ 401, 404 (Fed. Cir. 1983); In re Lowry, 32 F.3d 1579, 32 USPQ2d 1031 (Fed. Cir. 1994).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention was made to use XML to store the data in Cooke.

The motivation for doing so would have been to allow the invention as disclosed to be used in various fields of endeavor as the data suggests (XML is a web based technology), thus such data does not alter how the invention functions and the subjective interpretation of the data does not patentably distinguish the claimed invention.

Claim 3 recites similar limitations to claim 2, thus is rejected for the same reasons as claim 2.

Claims 16, 17 recite the same limitations as claims 2-3 in light of the rejection for claim 15. Thus claims 16 and 17 are rejected for the same reasons as claims 2-3.

Claim 25 recites similar limitations as claim 2, thus is rejected for the same reasons as claim 2.

Claim 33 recites similar limitations as claim 2, thus is rejected for the same reasons as claim 2.

Claim 5 is considered to be mere duplication of parts from claim 1, thus is rejected on the same grounds as claim 1. Claim 5 recites the process according to claim 1, further comprising identifying a *second* allowed programmable hardware resource. Identifying the second allowed programmable hardware resource is considered to be mere duplication of parts and has no patentable significance unless a new and unexpected result is produced. See MPEP §2144.04(B)

Regarding claim 6, the combination as applied to claim 5 teaches those limitations, In particular Cooke further teaches comprising highlighting the second allowed programmable hardware resource using said graphical user interface

> [The block floorplanner 120 provides for the definition of block functions, block regions, and constraints on these for the purpose of interactive floorplanning operations by the circuit designer, and the control of placement operations of the block placer 130. The block placer 130 determines the placement of cells within blocks according to the constraints defined by the circuit designer. (Paragraph 38)]" as claimed.

Regarding claim 9, Cooke teaches the method according to Claim 8.

Cooke does not expressly teach that the disallowed programmable resource is highlighted in gray.

However, this limitation is deemed to be obvious to a person of ordinary skill in the art, thus Examiner takes Official Notice that highlighting the disallowed

programmable resource in grey is well known in the art at the time of Applicant's invention.

The motivation for doing so would have been to visually indicate to the user that the placement was not acceptable.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. See PTO form 892.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Luke Osborne whose telephone number is (571) 272-4027. The examiner can normally be reached on 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Leo P. Picard can be reached on (571) 272-3749. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LRO

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